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|---|---|
| GARCIA, JOANNIE A | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Paper No. 20

Application Number: 09/728,554
Filing Date: December 01, 2000
Appellant(s): SHIELDS ET AL.

MAILED
AUG 1 8 2003
GROUP 2800

Deborah L. Corpus
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 05-30-03.

***(1) Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

*(2) Related Appeals and Interferences*

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

*(3) Status of Claims*

The statement of the status of the claims contained in the brief is correct.

*(4) Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

*(5) Summary of Invention*

The summary of invention contained in the brief is correct.

*(6) Issues*

The appellant's statement of the issues in the brief is correct.

*(7) Grouping of Claims*

Appellant's brief includes a statement that claims 1, 2, and 5-14 stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

*(8) Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

*(9) Prior Art of Record*

| | | |
|---|---|---|
| 5,329,482 | NAKAJIMA ET AL | 7-1994 |

*(10) Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, and 5-14, are rejected under 35 U.S.C. 102(e) as being anticipated by Nakajima et al (U.S. Patent 5,329,482).

Nakajima et al discloses depositing a first oxide layer 8 over at least two polysilicon lines 6 and 12 of each of a core and a periphery area (Abstract, and Column 5, lines 27-31), performing a first spacer etch in the core and periphery area, implanting an area 11 located between two polysilicon lines in the core area (Column 5, lines 36-39), applying a second oxide layer 9 over the core and periphery areas (Column 5, lines 28-29), and performing a second spacer etch over the periphery area wherein a different appearance of the core and periphery area is produced (Figure 5). Nakajima et al also teaches that the first oxide layer has a thickness of less than one-half the distance between a periphery of the adjacent polysilicon lines (Figure 5). Nakajima et al is disclosing as well, performing a second spacer etch over the core area, and that the implanting 11 of an area occurs after the performing of the first spacer etch (Figure 5). Nakajima et al is also teaching implanting of an area located between at least two polysilicon lines in the periphery area, and that said implantation 14 occurs after the performing of the first spacer etch. Nakajima et al teaches as well, implanting of an area located between at least two polysilicon lines in the core area occurs after the performing of the second spacer etch.

Nakajima et al teaches forming an electronic component and forming a second spacer 9 adjacent at least one first spacer 8 (Figure 5).

*(11) Response to Argument*

Appellant argues that Nakajima et al fails to disclose depositing a first oxide layer over at least two adjacent polysilicon lines in each of a core area and a periphery area, that two polysilicon lines are in the same area, and implanting an area located between at least two adjacent polysilicon lines in the core area, therefore doping between adjacent polysilicon lines in the same area to form sources and drains, the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines. However, Nakajima et al depicts only one transistor in each region for the sake of simplicity and it refers to only one memory cell transistor repeatedly, also as an example, even though plural memory cells with their associated peripheral transistor are disclosed (Column 1, lines 28-49). Furthermore, Nakajima et al discloses depositing plural gate electrodes with their respective LDD structures in the memory area and the periphery area (Column 1, lines 36-49), and formation of a memory section and a periphery section on the same substrate with their respective MOS transistors (Column 2, lines 64-66).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

JAG
August 7, 2003

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